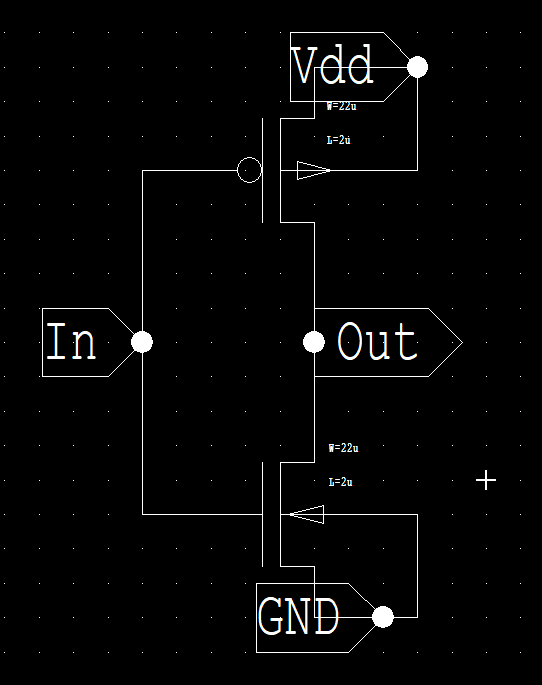
Digital IC Lab

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**Assignment 1: CMOS Inverter Characteristics**

# Inverter schematic:

****

# Transient Response:

## Output:

# DC Sweep:

## Output:

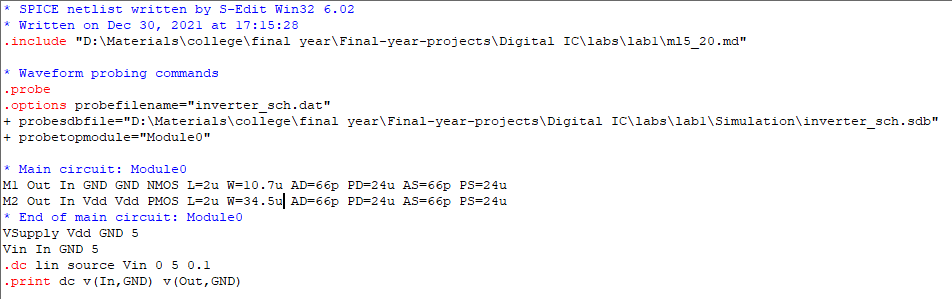
## Comment:

We notice that Vth = 2.03 V when VDD = 5 V, NMOS has L=2u W=22u and PMOS has L=2u W=22u

# Requirements:

## resize transistors to get matching inverter Vth = Vdd/2 (this is done by DC sweep

We resized the transistors by trials until getting the matching inverter where Vth = 2.5 V which is VDD/2, and thus where,

* NMOS has L=2u W=10.7u
* PMOS has L=2u W=34.5u

## Output:

## resize transistors to ensure ꞆPhl = ꞆPlh, also measure the max frequency (this is done by transient analysis)

## Output:

## Getting ꞆPhl and ꞆPlh:

### ꞆPhl 4.93us

### ꞆPlh 4.91us

Then, ꞆPhl ꞆPlh

## With a Capacitor of 1pF added

## Output:

## Getting ꞆPhl and ꞆPlh:

### ꞆPhl 4.97us

### ꞆPlh 4.95us